Dr. Soumya Pandit

Associate Professor | Institute of Radio Physics and Electronics | University of Calcutta

Kolkata, India • sprpe@caluniv.ac.in • +91 9874852007 • drsoumyapandit.in

Academic Profile

Academic in **VLSI Design and Microelectronics**, specializing in analog IC design, ultra-low-power circuits, semiconductor device modeling, process variability and EDA. **Ph.D., IIT Kharagpur (2009)**; Associate Professor, University of Calcutta (since 2020). Contributions span **indigenous semiconductor chip development, research infrastructure, nationally funded programmes, industry-oriented VLSI education and international IEEE leadership**.

Major Academic Contributions and Achievements

- **National Semiconductor Recognition | SEMICON India 2025:** Two University of Calcutta–designed chips (C2S0001 and C2S0048), fabricated under the MeitY Chips to Startup programme, featured in the Made-in-India chip collection presented to the Hon'ble Prime Minister of India.
- **Semiconductor Research Infrastructure**: Established the ASIC Design Laboratory and SCL 180 nm CMOS design-to-tapeout capability at the University of Calcutta, enabling indigenous chip development and postgraduate research.
- **National Research Programme Leadership:** Chief Investigator of MeitY-funded SMDP–C2SD and Chips to Startup (C2S) programmes; Principal Investigator of sponsored projects in analog design automation and semiconductor device–circuit co-design.
- **Curriculum Innovation and Industry Collaboration:** Contributed to industry-aligned revision of the M.Tech. VLSI Design curriculum and promoted student training through engagement with HCL Technologies, TSMC and the VLSI Society of India (1TOPS initiative).
- **International Professional Leadership:** Editor-in-Chief, IEEE Electron Devices Society Newsletter; former Vice Chair, IEEE EDS Region 10 SRC, and Chair, IEEE EDS Calcutta Chapter. Fellow, IE(I) and IETE.
- **Academic and Institutional Leadership:** Former Coordinator of M.Tech. VLSI Design programmes (Regular and Working Professionals); Coordinator, Centralized Technology Internship Cell (CTIC), IIC- University of Calcutta.
- **Research and Scholarly Contributions:** Author of a CRC Press research monograph and 30 journal publications, 14 book chapters, 35 conference publications. Research supervision includes 5 doctoral scholars (2 awarded, 2 submitted thesis and 1 enrolled) and more than 25 postgraduate dissertations. **Google Scholar:** h-index: 9 | i10-index: 8 | Total citations: 227
- **Institutional Digital Innovation:** Developed IPMS and CTIC ERP platforms for research project management, internship administration, financial workflows and institutional process automation for C2S project and IIC-CU.

Education

Year	Degree	Institution
2009	Ph.D. in Engineering (VLSI Design)	Indian Institute of Technology Kharagpur
2002	M.Tech., Radio Physics and Electronics (First Class)	University of Calcutta
2000	M.Sc., Electronic Science (First Class)	University of Calcutta
1998	B.Sc. (Hons.), Physics (First Class)	University of Calcutta

Doctoral thesis: *"An Optimization-based Methodology for High-Level Design of Analog Systems."*

Academic and Professional Appointments

Period	Appointment / Institution
Feb 2020–present	Associate Professor, Institute of Radio Physics and Electronics, University of Calcutta
Feb 2017–Feb 2020	Assistant Professor, Stage III, University of Calcutta
Feb 2012–Feb 2017	Assistant Professor, Stage II, University of Calcutta
Nov 2008–Feb 2012	Assistant Professor, Stage I, University of Calcutta
Feb–Oct 2008	Assistant Professor, Meghnad Saha Institute of Technology
Aug 2003–Apr 2008	Research Consultant, SRIC, IIT Kharagpur
Jan 2002–Jul 2003	Lecturer, Meghnad Saha Institute of Technology

Research Areas

- Intelligent Analog IC Design and AI/ML-Assisted VLSI Optimization
- Ultra-Low-Power Analog Integrated Circuits
- Semiconductor Device Modeling and Process Variability
- FPGA-Based Intelligent Embedded Systems

Sponsored Research and Technology Development

Project title / funding agency	Role	Period	Grant amount	Status
1. Development of an Ultra-Low-Power Analog Front-End Circuit and Machine Learning-Assisted Processing Unit for Assessment of Air Filter Performance in an IAQM System *MeitY, Government of India — Chips to Startup (C2S) Programme*	Chief Investigator	2023–2028	₹84.62 lakh	**Ongoing**
2. Special Manpower Development Programme – Chip to Systems Design (SMDP–C2SD) in VLSI Design *MeitY, Government of India*	Chief Investigator	2015–2021	₹95.09 lakh, plus centrally procured EDA tools and servers	**Completed**
3. Modern Biology and Signal Processing Group *University with Potential for Excellence (UPE), University of Calcutta*	Principal Investigator	2017–2019	₹6.00 lakh	**Completed**
4. Development of a Design Automation Tool for Nano-CMOS Analog Circuits *DST, Government of India — Fast Track Young Scientist Scheme*	Principal Investigator	2010–2013	₹12.12 lakh	**Completed**
5. Device–Circuit Co-Design and Integration of Device CAD and Circuit CAD for the Study of Nanoscale MOS Transistors for Low-Power SoC Applications *Technical Education Quality Improvement Programme (TEQIP)*	Principal Investigator	Nov 2013–Nov 2015	₹1.00 lakh	**Completed**
6. Statistical Modeling, Design and Optimization of Nano-CMOS Analog/RF Circuits *Centre for Research in Nanoscience and Nanotechnology (CRNN), University of Calcutta*	Principal Investigator	2009–2011	₹2.00 lakh, plus salary of one SRF	**Completed**

Academic Leadership and Administrative Responsibilities

Position / Responsibility	Institution / Programme	Period
Coordinator, Centralized Technology Internship Cell (CTIC)	Institution's Innovation Council, University of Calcutta	May 2026–Present
Coordinator, M.Tech. VLSI Design Programmes	Regular and Working Professionals, University of Calcutta	Until Jan. 2026
Teacher-in-Charge, IC Design Laboratory	Institute of Radio Physics and Electronics, University of Calcutta	Ongoing
Member, Board of Studies / Board of Postgraduate Studies	University of Calcutta	—
Member, Board of Studies	National Institute of Science and Technology, Berhampur under BPUT Odhisa	—
Member, Board of Studies	University of Burdwan	2026–Present
Member, Curriculum Revision Committees	B.Tech. ECE and M.Tech. VLSI Design, University of Calcutta	—
Member, Departmental Committee	Radio Physics and Electronics, University of Calcutta	—

Teaching and Pedagogical Contributions

Teaching Philosophy: Emphasis on conceptual clarity, design-oriented learning, practical competence and independent research.

- **Undergraduate Education:** Analog Circuits (Theory and Laboratory) and Circuit Theory Laboratory, integrating analytical problem-solving, simulation and experimental learning.
- **Postgraduate Education:** Microelectronic Circuits, Analog IC Design, VLSI Testing and Verification, ASIC Design Laboratory, Reconfigurable Logic and SoC, and MEMS and Microsystems, emphasizing industry-standard EDA tools and design-to-silicon methodologies.
- **Doctoral Education:** Research Methodology and Scientific Writing using LaTeX, fostering critical thinking, independent investigation and effective scholarly communication.

10 Selected Representative Journal Publications

1. K. Mukherjee, A. Das, R. K. Pal and **S. Pandit**, "A High-Stability Sub-100 nW, First Order Tunable Gm-C Low-Pass Filter With 5.7 Hz/V Line Voltage-Sensitivity and 1.4 Hz/°C Thermal Drift," *International Journal of Circuit Theory and Applications*, vol. 54, no. 11, November 2026. DOI: 10.1002/cta.70592. Impact Factor: 1.4

2. K. Mukherjee, A. Das, R. K. Pal and **S. Pandit**, "An Ultra-Low Power, Highly Linear, Fully Differential Programmable Gain Amplifier With 0.017%/V Line Sensitivity and 50-mdB/°C Temperature Coefficient for Low-Frequency Applications," *International Journal of Circuit Theory and Applications*, vol. 54, no. 7, pp. 3982–3999, 2026. Impact Factor: 1.4

3. K. Mukherjee, R. K. Pal and **S. Pandit**, "A 0.41-μW Self-Biased Temperature and Offset-Compensated Fully Differential Instrumentation Amplifier With 47 mdB/°C Thermal Sensitivity and 425 pVolt/°C Offset Drift," *International Journal of Circuit Theory and Applications*, 2024. DOI: 10.1002/cta.4397. Impact Factor: 1.4

4. S. Banerjee, S. Chatterjee, K. Mukherjee and **S. Pandit**, "A 0.6 V voltage reference circuit with 57 ppm/°C temperature coefficient, 73 kΩ output impedance and 0.080%/V line sensitivity for energy efficient applications," *Physica Scripta*, vol. 99, no. 3, 2024. Impact Factor: 2.6

5. S. K. Maity and **S. Pandit**, "Modeling of inversion layer capacitance of III-V double gate MOSFETs using a neural network-based regression technique," *Journal of Computational Electronics*, vol. 22, pp. 1472–1481, 2023. Impact Factor: 2.8

6. K. Mukherjee, T. Sau, S. Upadhyay, S. Mitra, A. Bhowmik, S. Sarkhel, **S. Pandit** and R. K. Pal, "A 588 nW, 1 nA current reference circuit with extremely low (0.002%/V) line sensitivity over a wide supply voltage range and low temperature coefficient," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 35, no. 4, e2999, 2022. DOI: 10.1002/jnm.2999. Impact Factor: 2.0

7. S. K. Maity, A. Haque and **S. Pandit**, "Charge-Based Compact Drain Current Modeling of InAs-OI-Si MOSFET Including Subband Energies and Band Nonparabolicity," *IEEE Transactions on Electron Devices*, vol. 67, no. 6, pp. 2282–2289, 2020. DOI: 10.1109/TED.2020.2984578. Impact Factor: 3.6

8. S. Das, D. K. Das and S. Pandit, "A Global Routing Method for Graphene Nanoribbons Based Circuits and Interconnects," *ACM Journal on Emerging Technologies in Computing Systems*, vol. 16, no. 3, Article 31, pp. 1–28, 2020. DOI: 10.1145/3384214 Impact Factor: 2.3

9. S. Sengupta and **S. Pandit**, "Analysis of Drain Current Local Variability of an n-Channel EδDC MOSFET Due to RDD Considering Inversion Charge and Correlated Mobility Fluctuations," *IEEE Transactions on Electron Devices*, vol. 65, no. 4, pp. 1267–1275, 2018. DOI: 10.1109/TED.2018.2808299. Impact Factor: 3.6

10. S. Sengupta and **S. Pandit**, "Channel Profile Design of EδDC MOSFET for High Intrinsic Gain and Low VT Mismatch," *IEEE Transactions on Electron Devices*, vol. 63, no. 2, pp. 551–557, 2016. DOI: 10.1109/TED.2015.2507065. Impact Factor: 3.6

Annexure: Detailed Academic Record

A. Journal Publications

1. K. Mukherjee, A. Das, R. K. Pal and **S. Pandit**, "A High-Stability Sub-100 nW, First Order Tunable Gm-C Low-Pass Filter With 5.7 Hz/V Line Voltage-Sensitivity and 1.4 Hz/°C Thermal Drift" International Journal of Circuit Theory and Applications, vol. 54, no. 11, November 2026.
2. K. Mukherjee, A. Das, R. K. Pal and **S. Pandit**, "An Ultra-Low Power, Highly Linear, Fully Differential Programmable Gain Amplifier With 0.017%/V Line Sensitivity and 50-mdB/°C Temperature Coefficient for Low-Frequency Applications," International Journal of Circuit Theory and Applications, vol. 54, no. 7, pp. 3982–3999, July 2026.
3. A. Das, S. Chatterjee, S. Biswas and **S. Pandit**, "Hardware–software codesign in an SoC-FPGA platform to implement a fusion framework using reduced dual-stack convolutional autoencoder," Biomedical Signal Processing and Control, vol. 114, article 109306, April 2026.
4. S. Chatterjee, **S.Pandit** and A. Das, "Coupling of A Lightweight Model of Reduced Convolutional Autoencoder with Linear SVM Classifier to Detect Brain Tumours on FPGA", Expert Systems with Applications, Elsevier, vol. 290, 128444, 2025. [https://doi.org/10.1016/j.eswa.2025.128444] (IF: 7.5)
5. S. Das, A. Deb, D.K. Das and **S. Pandit**, Performance-aware routing optimization for graphene nanoribbon interconnects, Sādhanā , Springer, ISSN : 0973-7677, Vol/Page no 0973-7677, February 2025.
6. S. Das, D.K. Das and **S. Pandit**, Reducing delay and resistance of GNR based interconnect using insertion of buffers, Analog Integrated Circuits and Signal Processing, Springer, Volume 123, article number 6, (2025)
7. K.Mukherjee, R.K. Pal and **S.Pandit** , A 0.41-μW Self-Biased Temperature and Offset-Compensated Fully Differential Instrumentation Amplifier With 47 mdB/°C Thermal Sensitivity and 425 pVolt/°C Offset Drift , International Journal of Circuit Theory and Applications, Wiley, https://doi.org/10.1002/cta.4397, December 2024
8. S. Banerjee, S.Chatterjee, K .Mukherjee and **S.Pandit**, A 0.6 V voltage reference circuit with 57 ppm/°C temperature coefficient, 73 KΩ output impedance and 0.080%/V line sensitivity for energy efficient applications, Physica Scripta, IoP Science, Vol. 99, No 3 , 21 February 2024, 1-18
9. S.K.Maity and **S.Pandit**, Modeling of inversion layer capacitance of III-V double gate MOSFETs using a neural network-based regression technique, Journal of Computational Electronics, Volume 22, pages 1472–1481, August 2023
10. S.Das, D.K.Das and **S.Pandit**, A novel routing algorithm for GNR based interconnect considering area optimization, interconnect-reliability and timing issues, Analog Integrated Circuits and Signal Processing, Springer, Volume 116, pages 49–67, (2023)
11. S.K.Maity, P.Dutta and **S.Pandit**, 'Compact drain current modeling of planar InGaAs quantum well MOSFET', Micro and Nano Structures, Elsevier, Volume 169, September 2022, Date: 13.08.2022 Pages: 207361, 1-14, IF = 3.22, https://doi.org/10.1016/j.micrna.2022.207361
12. S.K.Maity and **S.Pandit**, 'Device-circuit analysis of ultra-thin body In1−xGaxAs on insulator MOS transistor with varying indium mole fraction and channel thickness', Engineering Research 8695/ac6ecc, Online ISSN: 2631-8695 Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II IF = 1.205
13. K.Mukherjee, T.Sau, S.Upadhyay, S.Mitra, A.Bhowmik, S.Sarkhel, **S.Pandit**, R.K.Pal, 'A 588 nW, 1 nA current reference circuit with extremely low (0.002%/V) line sensitivity over a wide supply voltage range and low temperature coefficient' International Journal of Numerical Modeling: Electronic Networks,

Devices and Field, John Willey and Sons, Date: 18.03.2022, https://doi.org/10.1002/jnm.2999, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, IF=1.054

14. S.K.Maity and **S.Pandit**, 'A SPICE compatible physics-based intrinsic charge and capacitance model of InAs-OI-Si MOS transistor'. Superlattices and Microstructures Page No: 106975: 1-13 Date: August 2021, Superlattices and Microstructures, Volume 156, August 2021, 106975, https://doi.org/10.1016/j.spmi.2021.106975 , ISSN: 0749-6036, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II IF = 2.658
15. S.Sengupta and **S.Pandit**, 'A Unified Model of Drain Current Local Variability due to Channel Length Fluctuation for an n-channel Eδ DC MOS Transistor', Silicon, Springer Vol 14, https://doi.org/10.1007/s12633-021-01218-w, Page No: 4979-4989, Date: 31.07.2021, Electronic ISSN 1876-9918, Print ISSN 1876-990X, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, IF = 2.941
16. S.K.Maity and **S.Pandit**, 'Performance Assessment of CMOS circuits using III-V on Insulator MOS Transistors', Silicon, Springer, Vol. 13, . https://doi.org/10.1007/s12633-020-00582- , Page No: 1939–1949, Date: 13.09.2020, Electronic ISSN 1876-9918, Print ISSN 1876-990X, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, IF = 2.941
17. S.K.Das, D.Das and **S.Pandit**, 'A Global Routing Method for Graphene Nanoribbons Based Circuits and Interconnects', ACM Journal on Emerging Technologies in Computing Systems Vol. 16 Issue 3 July 2020 https://doi.org/10.1145/3384214, Page No: 31:1-31:28 Date: 22.05.2020, ISSN:1550-4832, EISSN:1550-4840, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, IF = 1.420
18. S. K. Maity, A. Haque and **S. Pandit**, "Charge-Based Compact Drain Current Modeling of InAs- OI-Si MOSFET Including Subband Energies and Band Nonparabolicity," in IEEE Transactions on Electron Devices, vol. 67, no. 6, pp. 2282-2289, June 2020, doi: https://10.1109/TED.2020.2984578 Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, IF = 3.222
19. S.K.Maity and **S.Pandit**, 'Analysis of scaling of thickness of the buffer layer on analog/RF and circuit performance of InAs-OI-Si MOSFET using NQS model', International Journal of Numerical Modeling: Electronic Networks, Devices and Field, John Willey and Sons, Page no 1- 16, Date: 31.07.2019, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, IF:1.054, https://doi.org/10.1002/jnm.2664
20. S. Sengupta and **S. Pandit**, "Analysis of Drain Current Local Variability of an n-Channel E δ DC MOSFET Due to RDD Considering Inversion Charge and Correlated Mobility Fluctuations," in IEEE Transactions on Electron Devices, vol. 65, no. 4, pp. 1267-1275, April 2018, doi: https://10.1109/TED.2018.2808299 Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, IF = 3.222
21. S.K.Maity and **S.Pandit**, 'Effects of BOX Engineering on Analog/RF and circuit performance of InGaAs-OI-Si MOSFET', Page no 1777-1794, Date: 13th July 2017, International Journal of Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, IF=1.227
22. S.K.Maity and **S.Pandit**, Study of G-S/D underlap for enhanced analog performance and RF/circuit analysis of UTB InAs-OI-Si MOSFET using NQS small signal model, Superlattice and Microstructure, Elsevier, 2016. http://dx.doi.org/10.1016/j.spmi.2016.11.053 Page No: 362- 372, Date: 01.02.2017, ISSN: 0749-6036, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, IF = 2.658
23. R.Das, A.K.Gond, S.Sengupta and **S.Pandit**, Study of temperature variation on threshold voltage and sub-threshold slope of EδDC MOS transistor including quantum corrections and reduction Techniques, Microsystem Technologies, Springer, Vol. 23, No 9, 2017, DOI https://10.1007/s00542-016-2995-z , Page No: 4221–4229, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, IF = 2.658

24. S.Sengupta and **S.Pandit**, Substrate Bias Effect of Epitaxial Delta Doped Channel MOS Transistor for Low Power Applications, International Journal of Electronics, Taylor and Francis, UK, Vol. 104, No 1, ISSN 0020-7217 (Print); ISSN 1362-3060 (Online), Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, IF = 1.457, https://doi.org/10.1080/00207217.2016.1180546
25. S. Sengupta and **S. Pandit**, "Channel Profile Design of Eδ DC MOSFET for High Intrinsic Gain and Low VT Mismatch," in IEEE Transactions on Electron Devices, vol. 63, no. 2, pp. 551- 557, Feb. 2016, doi: https://10.1109/TED.2015.2507065, ISSSN No: 0018-9383, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, IF = 3.222
26. S.Sengupta and **S.Pandit**, Study of performance scaling of 22nm epitaxial delta-doped channel MOS transistor', International Journal of Electronics, Taylor and Francis, UK, 0020-7217 (Print), 1362-3060 (Online) , Page No: 967-981 Date: 12.08.2014, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II , IF = 1.457
27. J.Mukhopadhyay and **S.Pandit**, Modeling and Design of a Nano Scale CMOS Inverter for Symmetric Switching Characteristics, Volume 2012 | Article ID **475952** | https://doi.org/10.1155/2012/505983 Hindwai, Pages: 1-13 Date: 22.04.2012
28. **S.Pandit**, C. Mandal and A.Patra, A Methodology for Generation of Performance Models for the Sizing of Analog High-Level Topologies, VLSI Design, vol. 2012, Article ID 505983, Hidwai. ISSN: 1065-514X (Print), ISSN: 1563-5171 (Online) doi: https://10.1155/VLSI Pages: 1-1 Date: 15.09.2011,
29. **S.Pandit**, C.Mandal and A.Patra, An Automated High-Level Topology Generation Procedure for Continuous-Time ΣΔ Modulator', Integration, the VLSI journal, 2010, Vol. 43 Pages: 289- 304, Date: 04.03.2010
30. **S. Pandit**, S. K. Bhattacharya, C. Mandal and A. Patra, "A Fast Exploration Procedure for Analog High-Level Specification Translation," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 27, no. 8, pp. 1493-1497, Aug. 2008, doi: https://10.1109/TCAD.2008.925785. Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II IF: 2.565

B. Authored Book

1. **S.Pandit**, C.Mandal and A.Patra, Nano-Scale CMOS Analog Circuits: Models and CAD Techniques for High-Level Design, CRC Press, USA, Taylor & Francis, UK and others, 2014, Print ISBN: 978-1-4665-6426, eBook ISBN: 978-1-4665-6428-2

C. Book Chapters

1. **S. Pandit** and K. Mukherjee, "Low-Power Analog Amplifier Design using MOS Transistor in the Weak Inversion Mode," in Advanced Nanoscale MOSFET Architectures: Current Trends and Future Perspectives, Wiley-IEEE Press, 2024, pp. 255–280.
2. S. Das, A. Deb, **S. Pandit** and D. K. Das, "Obstacle-Aware Routing Algorithm for Graphene Nanoribbon Interconnects," in Next-Generation High-Speed Electronics and Optoelectronics, Lecture Notes in Electrical Engineering, 2025, pp. 213–236.
3. **S. Pandit**, Characterization of Stochastic Process Variability Effects on Nano-Scale Analog Circuits. In: Chapter in Book, Book Title Nanoelectronics for Next-Generation Integrated Circuits Edited By Rohit Dhiman, Taylor and Francis/CRC Press | 9781003155751
4. **S. Pandit**, Design Methodology for Ultra-Low-Power CMOS Analog Circuits for ELF-SLF Applications Page No: 23–43. In: Chapter in Book, Book Title Dhiman, R., Chandel, R. (eds) Nanoscale VLSI. Energy Systems in Electrical Engineering. Springer, Singapore. https://doi.org/10.1007/978- 981-15-7937-0_2 | Print ISBN 978-981-15- 7936-3 Online ISBN 978-981-15- 7937-0
5. A. Gond and **S. Pandit**, CMOS Design and Analysis of Four Quadrant Analog Multiplier Circuit for LF Applications Page No: 279–289 Date: 17.12.2019. In: Chapter in Book, Book Title: Lecture Notes in Electrical Engineering, vol 602, Springer, Singapore, Kundu, S., Acharya, U., De C., Mukherjee S. (eds)

https;//doi.org/10/1007/978-981-15- 0829-5_28. Date: 17.12.2019 | Print ISBN 978-981-15- 0828-8 Online ISBN 978-981-15- 0829-5

6. S.K. Maity and **S.Pandit,** UTB III-V-OI-Si MOS Transistor: the future transistor for VLSI Design Date: September 2019 Pages: 27-46. In: Chapter in Book, Book Title: VLSI and Post-CMOS Electronics, Edited by Rohit Dhiman, Rajeevan Chandel, IET, UK | ISBN-13: 978- 1-83953-053-1
7. M.Ghosh, S.Basu, **S.Pandit**, S.B. Mondal, Design of a Health Monitoring System for Heart Rate and Body Temperature Sensing Including Embedded Processing using ARM Cortex M3 Page No: 93-103. In: Chapter in Book, Book Title: Advances in Intelligent Systems and Computing, vol 999. Springer, Singapore, Das A., Nayak J., Naik B., Pati S., Pelusi D. (eds) | Print ISBN 978-981-13- 9041-8, Online ISBN 978-981-13- 9042-5
8. S.Basu, S.Sinha, **S.Pandit**, S.B. Mondal, Smart Health Monitoring System for Temperature, Blood Oxygen Saturation, and Heart Rate Sensing with Embedded Processing and Transmission Using IoT Platform, Page no: 81-92. In: Chapter in Book, Book Title: Advances in Intelligent Systems and Computing, vol 999. Springer, Singapore, Das A., Nayak J., Naik B., Pati S., Pelusi D. (eds) | Print ISBN 978-981-13- 9041-8, Online ISBN 978-981-13- 9042-5
9. S. Sengupta and **S.Pandit**, Variability in Nano-scale MOS Transistor and EδDC MOS Transistor Page no 25-48. In: Chapter in Book, Book Title: Nanoscale Devices: Physics, Modeling and their Application, Editor: B.K.Kaushik, Chapter 2, Publisher: CRC Press, USA, 16 November 2018 | ISBN: 9781138060340 eBook ISBN 978131516311 6
10. A.K.Gond, R.Gupta, S.Basu, **S. Pandit**, S.Barman, Behavioral Modeling of Differential Inductive Seismic Sensor and Implementation of its Read Out Circuit, Pages 253-262. In: Chapter in Book, Book Title: Communication, Devices, and Computing, Editor: Jaydeb Bhaumik Indrajit Chakrabarti Bishnu Prasad De Banibrata Bag Surajit Mukherjee, Springer Lecture Notes in Electrical Engineering, Vol. 470, April 2018. Publisher: Springer | ISBN 978-981- 10-8585-7
11. **S.Pandit**, Nanoscale MOSFET: MOS Transistor as Basic Building Block Page: 145–172 Date: 02.09.2015. In: Chapter in Book, Book Title: Introduction to Nano: Basics to Nanoscience and Nanotechnology, 2015 Publisher: Springer, Editor A.Sengupta and C.K.Sarkar. | ISBN 978-3- 662-47314-6
12. S.paul, A.Dana and **S.Pandit**, An Improved gm/ID Methodology for Ultra-Low-Power Nano-Scale CMOS OTA Design Pages: 128–137 Date: 2013. In: Chapter in Book, Book Title: Manoj Singh Gaur Mark Zwolinski Vijay Laxmi Dharmendra Boolchandani Virendra Singh Adit D. Singh (Eds.), CCIS 382, pp. 128–137, 2013. Publisher: Springer-Verlag Berlin Heidelberg 2013 | ISSN 1865- 0929 e-ISSN 1865-0937 ISBN 978-3- 642-42023-8 e- ISBN 978-3- 642-42024-5 DOI 10.1007/978-3- 642-42024-5
13. S.Sengupta and **S.Pandit**, Statistical Characterization of Flicker Noise Fluctuation of a Nano-Scale NMOS Transistor Page no 203-214 https://doi.org/10.1007/978-3-642- 34216-5_21. In: Advanced Nanomaterials and Nanotechnology Editor: P.K.Giri et al Publisher: Springer-Verlag Berlin Heidelberg 2013 | ISBN No: 978- 3-642-34215-8
14. **S.Pandit**, MOSFET Characterization for VLSI Circuit Simulation Page no: 267-362. In: Technology Computer Aided Design: Simulation for VLSI MOSFET Editor: Chandan Kumar Sarkar Publisher: CRC Press, USA, May 2013 | ISBN No: 978-1-4665- 1265-8

D. Conference Publications

1) S. Das, D. K. Das and **S. Pandit**, “Reduction of Interconnect Delay and Resistance While Minimizing Grid Area in GNR-Based VLSI Routing Problem,” in *Emerging Electronic Devices, Circuits and Systems*, Springer, 2022, pp. 85–97.
2) S. Das, D. K. Das and **S. Pandit**, “Reliability-Aware Global Routing of Graphene Nanoribbon-Based Interconnect,” in *Proceedings of the 26th International Symposium on VLSI Design and Test (VDAT)*, Springer, 2022, pp. 373–386.

3) S. Upadhyay, T. Sau, S. Mitra, A. Bhowmik, S. Sarkhel and **S. Pandit**, "Statistical Analysis of a Low Power Analog Current Source," in *Proceedings of the IEEE VLSI Device, Circuit and System Conference (VLSI DCS)*, 2022, pp. 160–164. DOI: 10.1109/VLSIDCS53788.2022.9811473.
4) T. Saquib, S. Sarkhel and **S. Pandit**, "A 0.6 V 1.6 nA Constant Current Reference Circuit with Improved Power Supply Sensitivity," in *Proceedings of the IEEE Devices for Integrated Circuit Conference (DevIC)*, 2021, pp. 498–503. DOI: 10.1109/DevIC50843.2021.9455885.
5) S. Das, P. Fišer, **S. Pandit** and D. K. Das, "Minimization of Switching Activity of Graphene Based Circuits," in *Proceedings of the 34th International Conference on VLSI Design and 20th International Conference on Embedded Systems*, IEEE, 2021, pp. 139–144. DOI: 10.1109/VLSID51830.2021.00029.
6) R. Aditya, S. Sarkhel and **S. Pandit**, "Comparative Study of Doublet OTA Circuit Topologies Operating in Weak Inversion Mode for Low Power Analog IC Applications," in *Proceedings of IEEE VLSI Device, Circuit and System Conference (VLSI DCS)*, 2020, pp. 74–78. DOI: 10.1109/VLSIDCS47293.2020.9179858.
7) S. Das, **S. Pandit** and D. K. Das, "Crosstalk Aware Global Routing of Graphene Nanoribbon Based Circuits," in *Proceedings of the IEEE 19th International Conference on Nanotechnology (IEEE-NANO)*, 2019, pp. 243–248. DOI: 10.1109/NANO46743.2019.8993935.
8) S. K. Maity and **S. Pandit**, "Compact Drain Current Modeling of InAs-OI-Si MOS Transistor Including Quantum Confinement," in *Proceedings of the International Symposium on Devices, Circuits and Systems (ISDCS)*, IEEE, 2018, pp. 1–5. DOI: 10.1109/ISDCS.2018.8379654.
9) K. Gond, S. Basu, S. Barman and **S. Pandit**, "Design and Analysis of a CMOS Analog Multiplier as Part of Readout Circuit for a Differential Inductive Seismic Sensor," in *Proceedings of the International Conference on Computing, Communication and Sensor Networks (CCSN)*, 2017, pp. 1–6.
10) S. Sengupta and **S. Pandit**, "Study of LER/LWR Induced Threshold Voltage Variability of an EδDC n-Channel MOS Transistor," in *Proceedings of IEEE Devices for Integrated Circuit Conference (DevIC)*, 2017, pp. 685–689.
11) S. K. Maity and **S. Pandit**, "Study of Short Channel Characteristics of Gate Underlapped InGaAs-OI-Si MOS Transistor," in *Proceedings of the National Conference on Devices and Circuits (NCDC)*, 2016.
12) S. K. Maity and **S. Pandit**, "Effect of Buried Oxide (BOX) Thickness Scaling on Analog/RF Performance of InGaAs-on-Insulator MOS Transistor," in *Proceedings of the 2nd International Conference on Microelectronics, Circuits and Systems*, 2015.
13) S.Sengupta and **S.Pandit**, "Temperature Analysis of Threshold Voltage and Sub-threshold Slope of Epitaxial Delta Doped Channel MOS Transistor for SoC Applications," in *Proceedings of the 2nd International Conference on Microelectronics, Circuits and Systems*, 2015, pp. 105–109.
14) M. Dutta, **S. Pandit** and S. Barman, "Amino Acid Classification Based on Electrical Response of Its Codon Composition," in *Proceedings of the IEEE International Conference on Research in Computational Intelligence and Communication Networks*, 2015, pp. 279–284.
15) R. Das, S,Sengupta and **S.Pandit**, "Study of Wide Temperature Variation (100–500 K) on Drain Current Characteristics of a 22 nm n-Channel EδDC MOS Transistor," in *Proceedings of the 4th International Conference on Computing, Communication and Sensor Networks*, 2015.
16) S. K. Maity and **S. Pandit**, "Impact of Gate Underlap on Analog/RF Performance of InGaAs-OI-Si Substrate MOS Transistor for SoC Computing Applications," in *Proceedings of the 4th International Conference on Computing, Communication and Sensor Networks*, 2015.
17) S. K. Maity and **S. Pandit**, "Study of Analog and RF Performance of UTB-OI-Si Substrate MOS Transistor Using Buffered InGaAs and Silicon Channel," in *Proceedings of the 6th International Conference on Computers and Devices for Communication (CODEC)*, IEEE, 2015, pp. 1–4.
18) Das, M. Ghosh, P. Banerjee and **S. Pandit**, "Power Aware Clustering and Placement for FPGAs," in *Proceedings of the 1st International Science and Technology Congress (IEMCON)*, 2014.

19) D. Bairagi and **S. Pandit**, “Study of Reverse Substrate Bias Effect of 22 nm Node Epitaxial Delta Doped Channel MOS Transistor for Low Power SoC Applications,” in *Proceedings of the 18th International Symposium on VLSI Design and Test (VDAT)*, IEEE, 2014, pp. 1–6.

20) S. Sengupta and **S. Pandit**, “Threshold Voltage Modeling of Deeply Depleted Channel MOSFET and Simulation Study of Its Analog Performances,” in *Proceedings of the International Conference on Electronics, Communication and Instrumentation (ICECI)*, IEEE, 2014, pp. 1–4.

21) S. Sengupta and **S. Pandit**, “Semi-Analytical Estimation of Intra-Die Variations of Analog Performances of Nano-Scale NMOS Transistor,” in *Proceedings of the 16th International Workshop on Physics of Semiconductor Devices (IWPSD)*, SPIE, vol. 8549, 2012, Article 854904, pp. 1–5.

22) D. Dhabak and **S.Pandit** “Performance Modeling of Nano-Scale CMOS Inverter Circuit Using Least Square Support Vector Machine,” in *Proceedings of the International Conference on Nanotechnology and Biosensors (ICNB)*, 2011, pp. 61–64.

23) S.Sengupta and **S.Pandit**, “Effects of Intra-Die Process Variations on Nano-Scale CMOS Analog Circuit Performances,” in *Proceedings of the International Conference on Nanotechnology and Biosensors (ICNB)*, 2011, pp. 165–168.

24) S.Sengupta and **S.Pandit**, “An Analytical Approach for Statistical Modeling of the Effect of Process Parameter Variation on the Performance of Nano-Scale CMOS VCO,” in *Proceedings of the International Conference on Future Applications of Nanotechnology (ICFANT)*, Jadavpur University, Kolkata, 2010, pp. 18–27.

25) S. Sengupta and **S. Pandit**, “Statistical Study of the Effect of Process Variations on Nano-Scale CMOS Circuits with Scaling,” in *Proceedings of the IEEE Annual India Conference (INDICON)*, 2010, pp. 1–4. DOI: 10.1109/INDCON.2010.5712724.

26) D. Dhabak and **S. Pandit**, “An Artificial Neural Network-Based Approach for Performance Modeling of Nano-Scale CMOS Inverter,” in *Proceedings of IEMCON*, 2011, pp. 165–170.

27) J. Mukhopadhyay and **S. Pandit**, “Design of a Nano-Scale CMOS Inverter with Symmetric Switching Characteristics Using Particle Swarm Optimization Algorithm,” in *Proceedings of IEMCON*, 2011, pp. 536–540. Authorship sequence provisional.

28) **S.Pandit,** C.R. Mandal and **A.Patra**, “A Methodology for Sizing of Analog High-Level Topologies Using Computational Intelligence Techniques,” in *Proceedings of the International Conference on Emerging Trends in Engineering Technologies (ICETES)*, Noorul Islam University, 2010, pp. 520–523. **Best Paper Award.**

29) S. Mandal and **S. Pandit**, “Statistical Simulation and Modeling of Nano-Scale CMOS VCO Using Artificial Neural Network,” in *Proceedings of the 24th International Conference on VLSI Design*, IEEE, 2011, pp. 94–99. DOI: 10.1109/VLSID.2011.28.

30) **S. Pandit**, C. Mandal and A. Patra, “Systematic Methodology for High-Level Performance Modeling of Analog Systems,” in *Proceedings of the 22nd International Conference on VLSI Design*, IEEE, 2009, pp. 361–366.

31) **S. Pandit**, C. Mandal and A. Patra, “A Hybrid Search Procedure for System-Level Analog Design Space Exploration Used in High-Level Synthesis of Analog Systems,” in *Proceedings of the International Conference on Computers and Devices for Communication (CODEC)*, 2006, pp. 114–117.

32) **S. Pandit**, C. Mandal and A. Patra, “A Formal Approach for High-Level Synthesis of Linear Analog Systems,” in *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, 2006, pp. 345–348.

33) **S. Pandit**, S. Kar, C. Mandal and A. Patra, “High-Level Synthesis of Higher-Order Continuous-Time State Variable Filters with Minimum Sensitivity and Hardware Count,” in *Proceedings of the Design, Automation and Test in Europe Conference (DATE)*, 2006, pp. 1203–1204.

34) **S. Pandit**, C. Mandal and A. Patra, “High-Level Synthesis of Linear Analog Systems,” in *Proceedings of the International Conference on Emerging Applications of Information Technology (EAIT)*, 2005, pp. 389–392. Conference title expansion requires confirmation.

35) **S.Pandit**, A. Addya, C.Pramanik, H.Saha “Porous Silicon Device Modeling and Linearization Technique,” in *Proceedings of the IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, 2003, pp. 145–148.

E. Ph.D. Research Supervision

1. Mrs. Sarmista Sengupta — Degree awarded: Thesis Title: Study of Process Variability Effects on EδDC MOS Transistor for Low Power VLSI Applications
2. Mr. Subir Maity — Degree awarded: Thesis Title: Studies on Device and Circuit Performance of III-V-OI-Si MOS Transistors
3. Mr. Subrata Das — Thesis Submitted: Optimized Routing Algorithms For VLSI Circuits Using Graphene Nanoribbon (GNR) Based Interconnects
4. Mrs. Koyel Mukherjee — Thesis Submitted: Design And Analysis Of Low Frequency CMOS-Based Analog Circuits Over A Wide Range Of Temperature Variation.
5. Miss. Tanusree Dutta — Enrolled

F. Postgraduate Dissertations

1. Saroj Mondal — E123_Core Micro-Architecture (2009)
2. Sipra Mandal — Modeling, Simulation and Design of a Nano-scale CMOS Circuits using Soft Computing Techniques (2010)
3. Chandan Mukherjee — Statistical Study of the Variation of Process Parameters on the Performance of CMOS VCO and OPAMP Circuits (2010)
4. Kaustav Dasgupta — Design and Study of Digital Phase Locked Loop using nanoscale CMOS Technology (2010)
5. Krishnendu Dey — Design of a Wide-band, Low-Power Digital Phase Locked Loop using 32-nm CMOS Technology (2010)
6. Dipankar Dhabak — Performance Modeling of Nano-scale CMOS Logic Circuits using Soft Computing Techniques (2011)
7. Joyjit Mukherjee — Design of a Nano-scale CMOS Inverter Circuits using Soft Computing Techniques (2011)
8. Debabrata Bose — Design of a nano-scale CMOS Inverter using Generic Algorithm. (2011)
9. Somnath Paul — Design of Amplifier for Ultra-Low Power Analog Application using nano-scale MOS Transistors (2012)
10. Abhijit Dana — SPICE Modeling and Parameter Extraction of Nano-scale MOS Transistors for Low Power Analog Circuit Applications (2012)
11. Pranjal Barman — Statistical Study of Random Discrete Dopant Effect in Scaled MOS Transistor and Its Reduction by Channel Engineering Approach (2012)
12. Kritanjali Das — Study of Analog Performances of Nano-scale MOS Transistors (2012)
13. DebayanBai ragi — Study of Substrate Bias Effect for Epitaxial Delta Doped Channel MOS Transistor (2014)
14. Aparna Das — Study of Power Aware Clustering for FPGA (2014)
15. Mousumi Ghosh — Study of Power Aware Placement for FPGA (2014)
16. Rahul Kumar Shaw — Design of a Low Power Front End OTA and PSO Application for the Optimization of Threshold Voltage Parameter of EδDC Transistor (2016)
17. Rinkee Das — Temperature Characterization over Wide Range (100-500K) of an n-channel EδDC MOS Transistor 2016)
18. Saswata Chatterjee — Design of a Low Frequency, Low Power, Fast Locking Digital Phase Locked Loop using SCL 180 nm technology (2017)
19. Suman Goswami — Adaptive Noise Cancellation of Seismic Signal using Least Mean Square Algorithm and Implementation using FPGA (2017)
20. Kaushik Sen — Modeling of a Differential Inductive Seismic Sensor and its Simulation using COMSOL Multiphysics (2017)
21. Monalisa Dutta — Design and Implementation of FPGA Based Earthquake Early Warning System (2017)
22. Sirsha Guha — Temperature Analysis of Device Performance of a sub-50nm p-channel FinFET (2019)
23. Srabanti Saha — Implementation of Multi-Phase DC-DC Bulk Converter (2020)
24. Sayantan Chanda — Evaluation of On-Chip Solution for Scan Bus Width Reduction on Large SoC (2021)
25. Anindita Das — Electromigration-aware Physical Design Automation of Multi- million Gate Chip (2021)
26. Raya Adhikary — Design of a Low Noise Instrumentation Amplifier for Sensor Applications (2022)

G. Invited Lectures, Keynote Addresses, Tutorials and Technical Talks

1. **Process Variability in Nano-Scale CMOS Analog Circuits** — Keynote Address, IEEE VLSI Device, Circuit and System Conference (VLSI DCS), IEEE EDS Student Branch Chapter, Meghnad Saha Institute of Technology, 26–27 February 2022.
2. **Variability in MOS Transistors** — 3rd International Conference on Devices and Circuits, Kalyani Government Engineering College, March 2019.
3. **Unified Model for Drain Current Local Variability in MOS Transistors** — 4th IEEE International Conference on Emerging Electronics, Bengaluru, 16–19 December 2018.
4. **Process Variability Modeling and Low-Leakage Device Design in IoT Design Space** — IEEE EDS Technical Talk, Department of Electrical Engineering, IIT Kanpur, 25 June 2018.
5. **Overview of Nano-Scale MOSFETs** — One-Day Seminar on Electron Devices and Applications, IEEE EDS Student Branch Chapter, Netaji Subhas Engineering College, 20 March 2018.
6. **VLSI Circuit Testing and Testability** — Invited Lecture, 4th National Conference on Devices and Circuits, NIST Berhampur, 24 February 2018.
7. **CMOS Analog IC Design** — Tutorial, Two-Day Workshop on Emerging VLSI Technologies, Assam University, Silchar.
8. **Epitaxial Delta-Doped Channel MOS Transistor: A Candidate for Smart Mobile SoC Applications** — Invited Lecture, 2nd International Conference on Microelectronics, Circuits and Systems, 11 July 2015.
9. **MOS Transistors for Advanced SoC Design** — Invited Lecture, International Workshop on Advanced Electron Devices and Circuits, IEEE EDS Calcutta Chapter and KIIT University, 3–4 December 2014.
10. **Short-Channel Effects in MOS Transistors** — Invited Lecture, Workshop on Advanced Semiconductor Device Modeling and Fabrication, Abacus Institute of Engineering and Management, 15 November 2014.
11. **Nano-Scale CMOS Analog Circuits: Essential Challenges and Design Methodologies** — Keynote Address, International Conference on Microelectronics, Circuits and Systems (MICRO 2014), Rourkela, 11 July 2014.
12. **Electron System Design and Manufacturing** — Invited Lecture, Seminar on Embedded Systems and VLSI, Elitte Institute of Engineering and Management, 29 March 2014.
13. **MOSFET Characterization for VLSI Circuit Simulation** — Faculty Development Programme on Recent Trends in VLSI Design and Embedded Systems, C. V. Raman College of Engineering, Odisha, 27 July 2012.
14. **Device Characterization for VLSI Circuit Simulation** — UGC-NRCPS Summer School, University of Calcutta, 1 June 2012.
15. **CMOS Analog Circuits** — UGC-NRCPS Summer School on Techniques for Design, Fabrication and Computation of Integrated Circuits (TECHNOMICS 2012), University of Calcutta, 29 May 2012.
16. **Low-Power CMOS Circuits** — UGC-NRCPS Summer School on Techniques for Design, Fabrication and Computation of Integrated Circuits (TECHNOMICS 2012), University of Calcutta, 2012.
17. **Interface Electronics for Smart Sensors** — UGC-NRCPS Winter School on Physics and Technology of Sensors (PHYTSENS 2012), University of Calcutta, 22 November 2012.
18. **MEMS Capacitive Sensors** — UGC-NRCPS Winter School on Physics and Technology of Sensors (PHYTSENS 2012), University of Calcutta, 26 November 2012.
19. **Performance Modeling, Parameter Extraction and Statistical Modeling of Nano-Scale CMOS Transistors for VLSI Circuit Simulation** — International Workshop on Device Modeling of Microsystems, MOS-AK/GSA and INAE, JIIT Noida, 16–18 March 2012.
20. **Low-Power CMOS Circuits** — Advances in Photonic, Electronic and Communication Systems (APECS 2012), Tezpur University, 24 January 2012.
21. **Parameter Extraction Techniques for MOS Modeling** — Academic Lecture, Advances in Electronics, Communication and Information Technology, Mizoram University, 25 March 2011.
22. **Low-Power CMOS Design: Sources and Minimization Techniques** — Academic Lecture, Advances in Electronics, Communication and Information Technology, Mizoram University, 24 March 2011.
23. **Statistical Modeling of Process Variability Effects on Nano-Scale CMOS Analog and RF Circuits** — IEEE Technical Talk, IEEE Calcutta Section, Electron Devices Society Chapter, 22 June 2010.
24. **CAD for Nano-CMOS Analog Design** — Frontiers of Electronics and Communication, North Eastern Regional Institute of Science and Technology (NERIST), Arunachal Pradesh, 8 September 2009.
25. **CMOS Device Modeling for Analog and Digital Circuits** — UGC-NRCPS Summer School (NanoDev), Institute of Radio Physics and Electronics, University of Calcutta, 3 June 2009.

H. Conference Leadership and Technical Service:

Served as Ph.D. Forum Chair (International Conference on VLSI Design, 2016), Technical Programme Committee Member for international conferences including VLSI Design, VLSI Design and Test, and Embedded Computing and System Design, and Session Chair at MICRO 2014, IEEE ICEE 2018 and OPTRONIX 2019.

Declaration

I hereby declare that the information furnished in this Curriculum Vitae is true, accurate and complete to the best of my knowledge and belief.

Dr. Soumya Pandit
Date:
Place: Kolkata